

FIG. 1

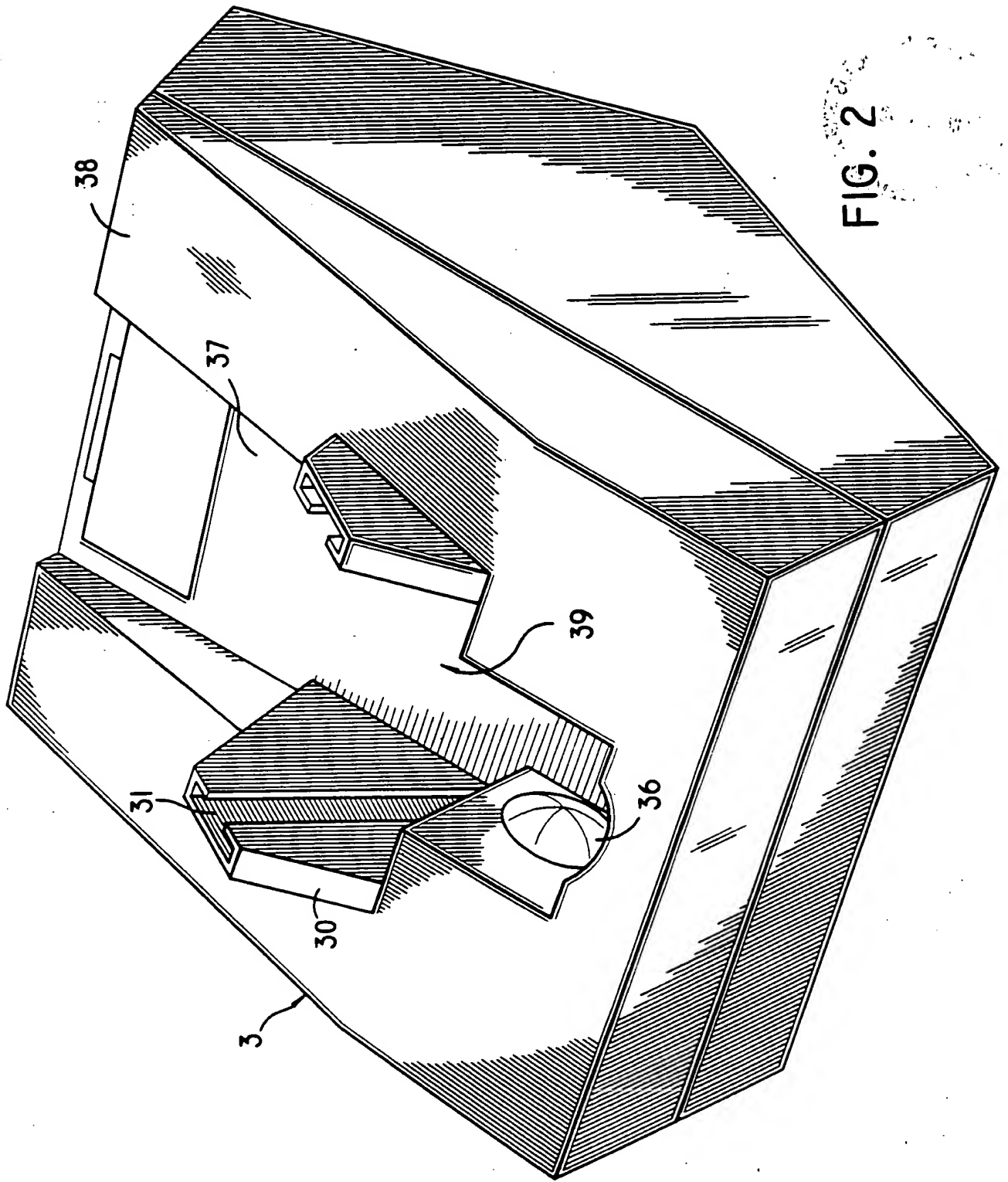


FIG. 2

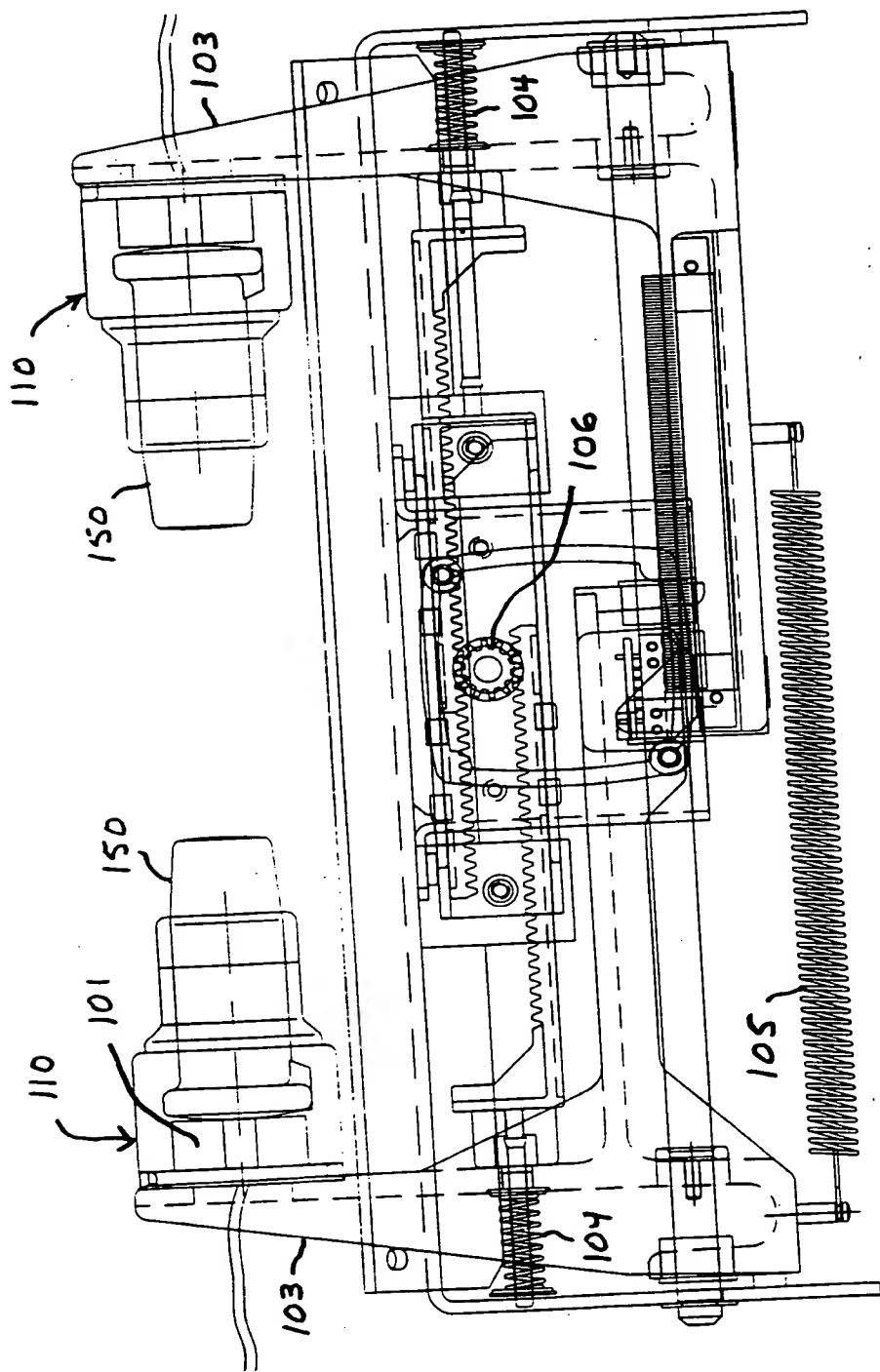


FIG. 3

FIG. 4A

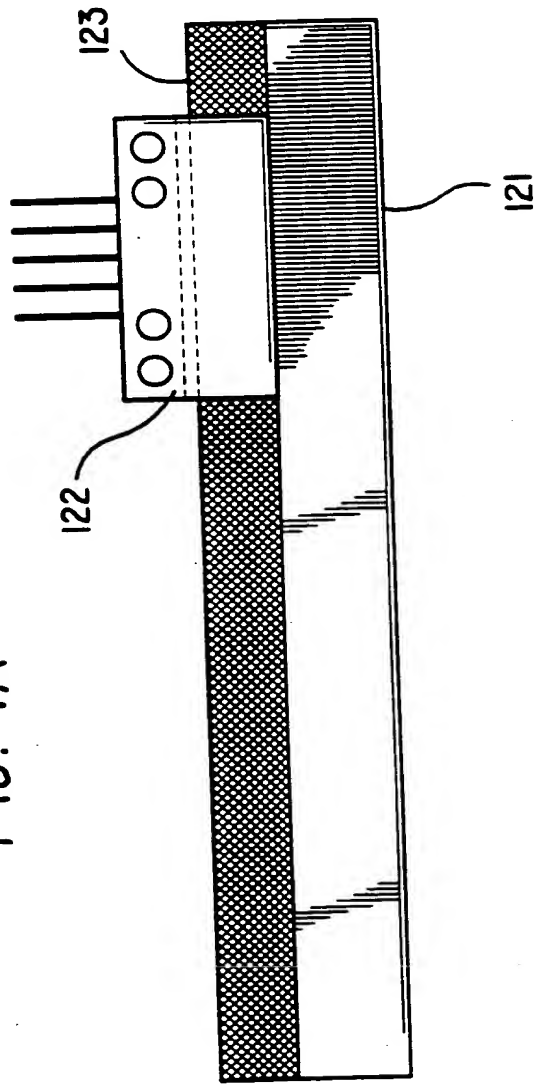


FIG. 4B

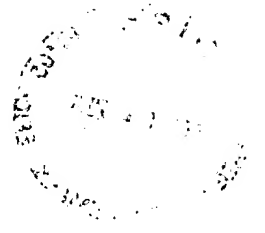
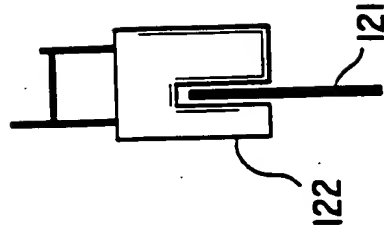
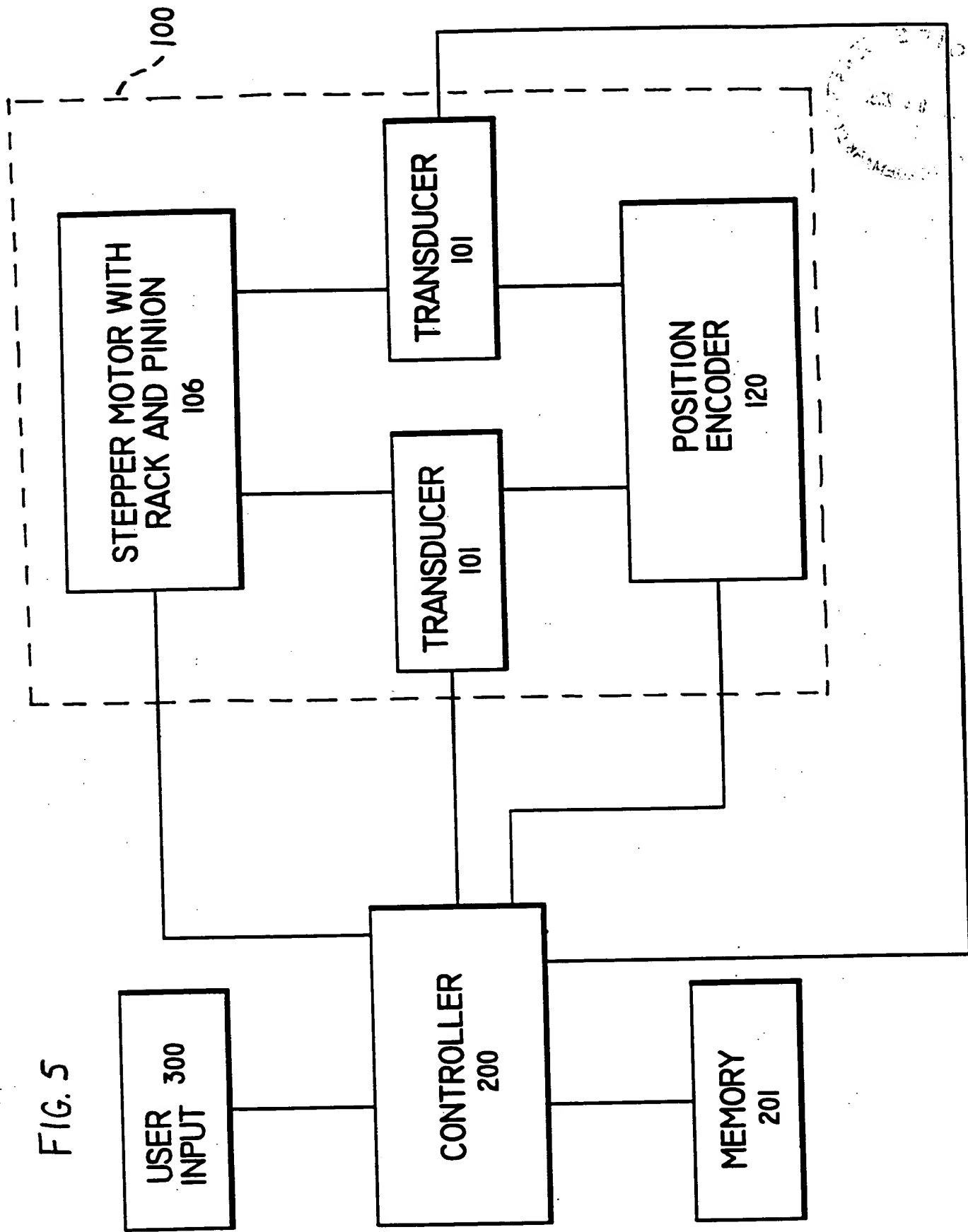


FIG. 5



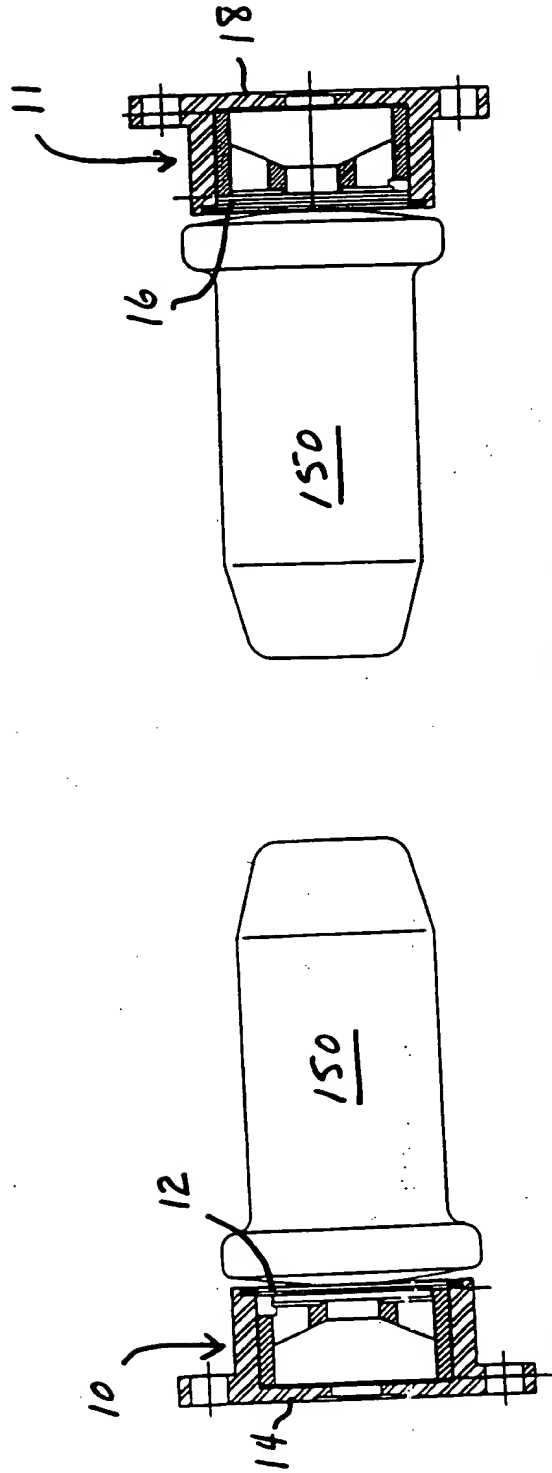


FIG. 6

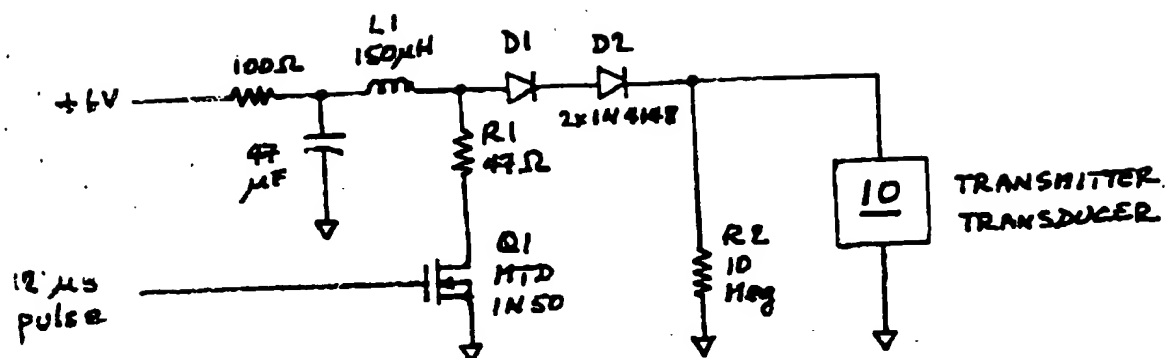


FIG. 7A

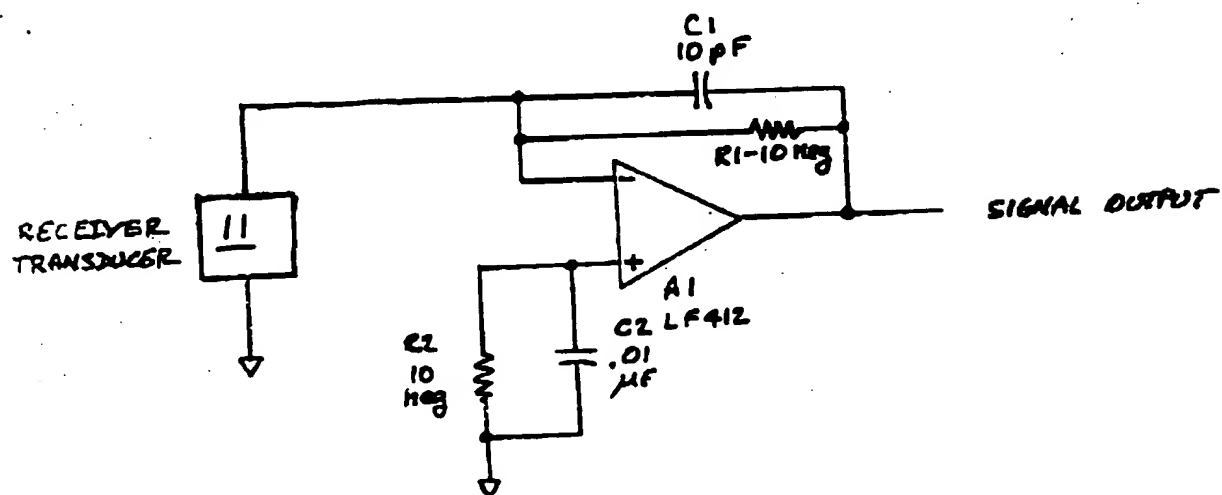


FIG. 7B

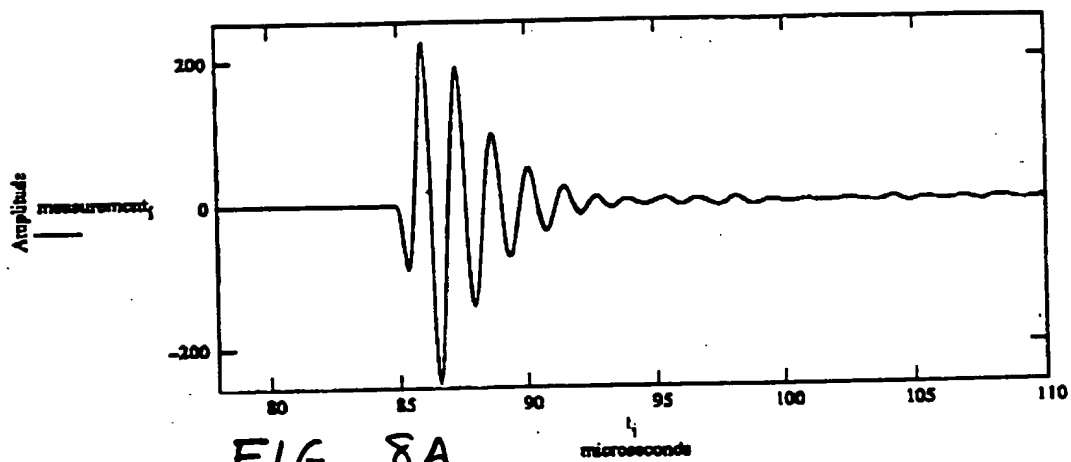


FIG. 8A

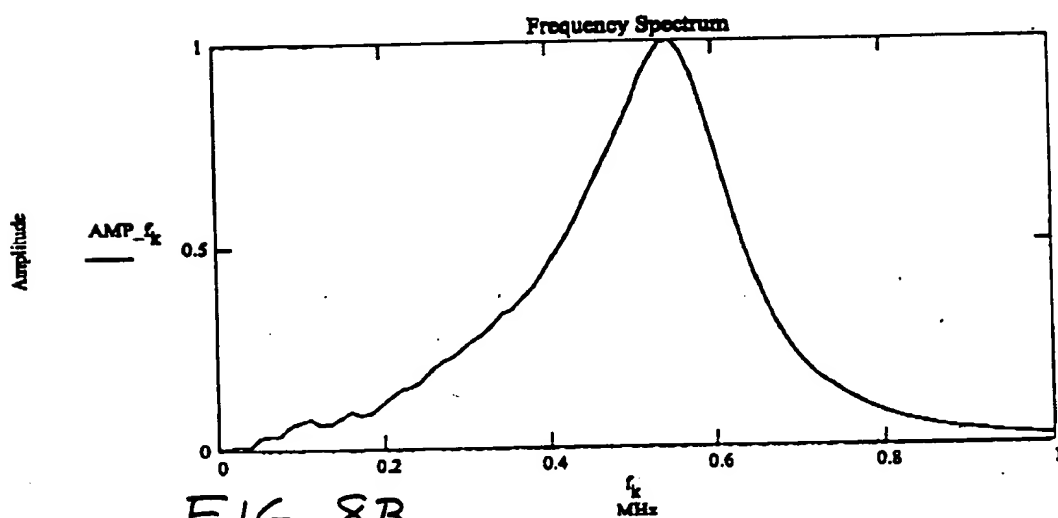


FIG. 8B

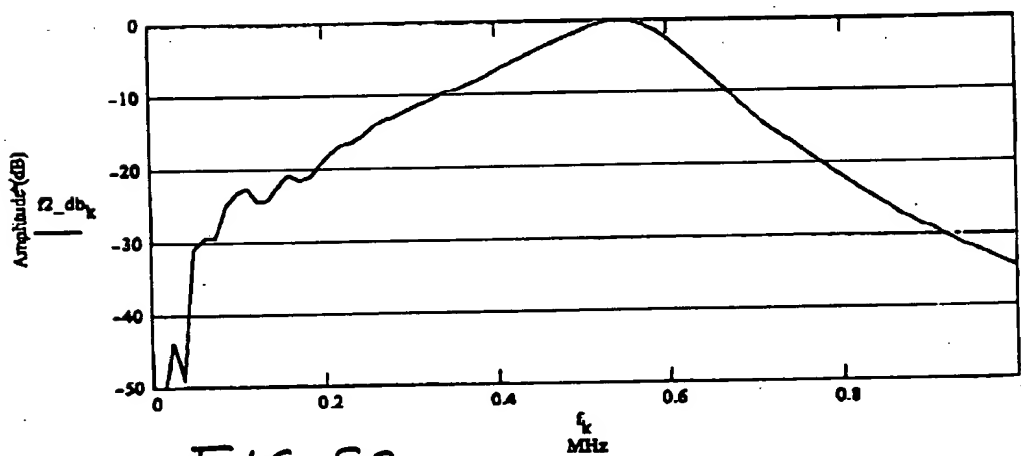


FIG. 8C

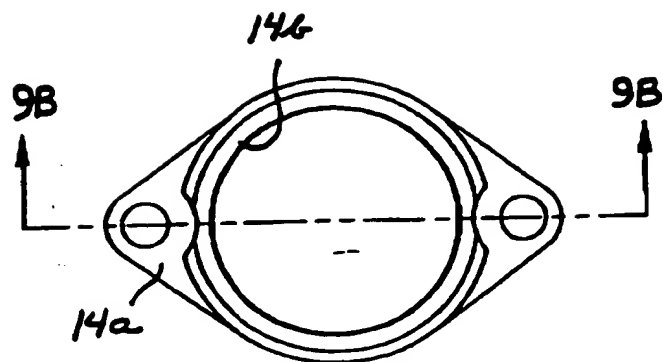


FIG. 9A

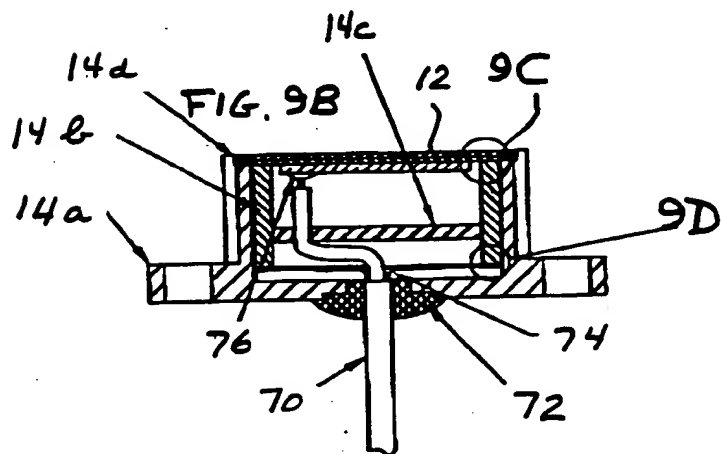


FIG. 9B

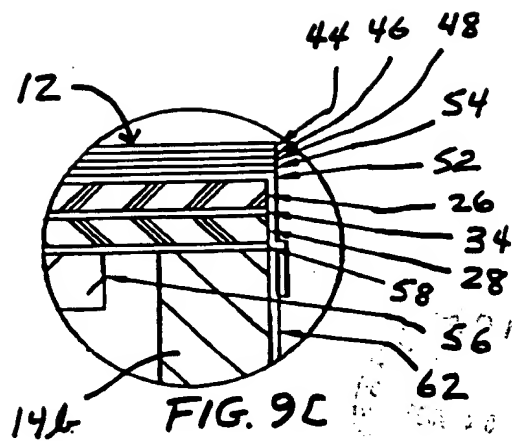


FIG. 9C

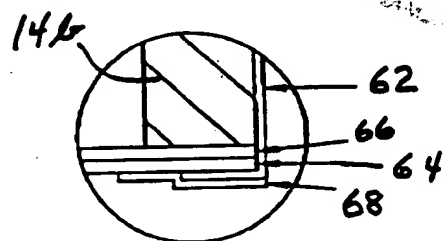


FIG. 9D

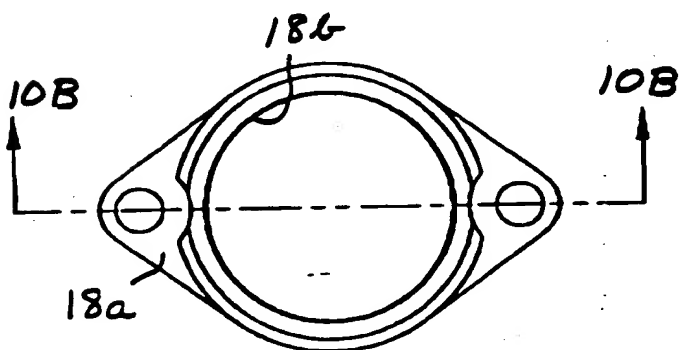


FIG. 10A

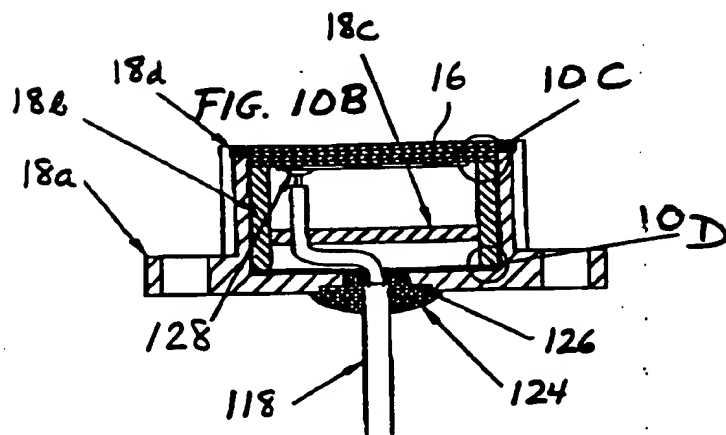


FIG. 10B

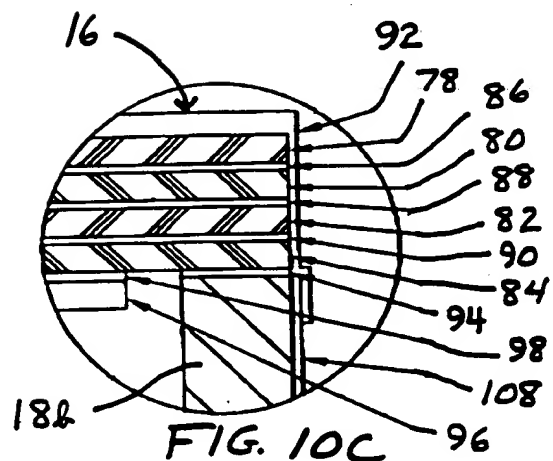


FIG. 10C

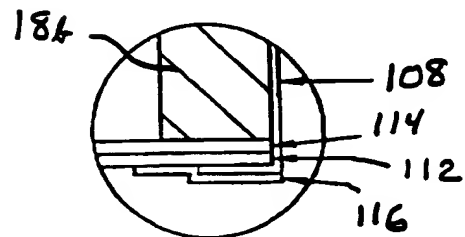
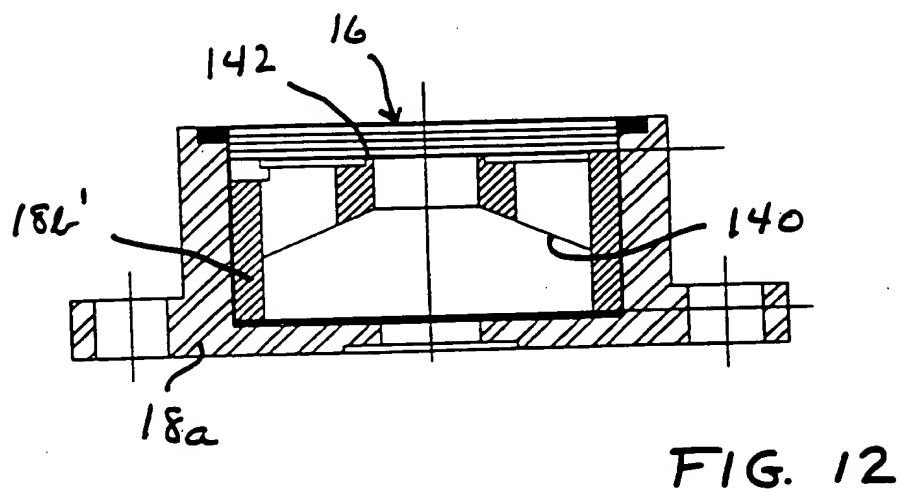
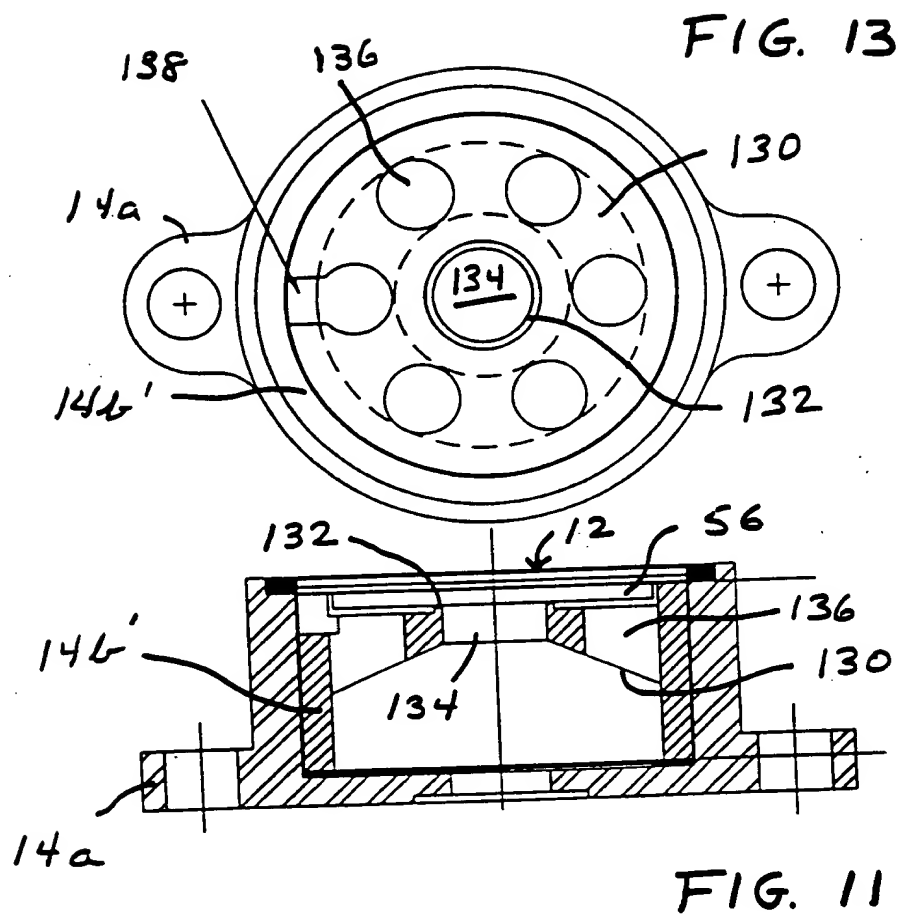


FIG. 10D



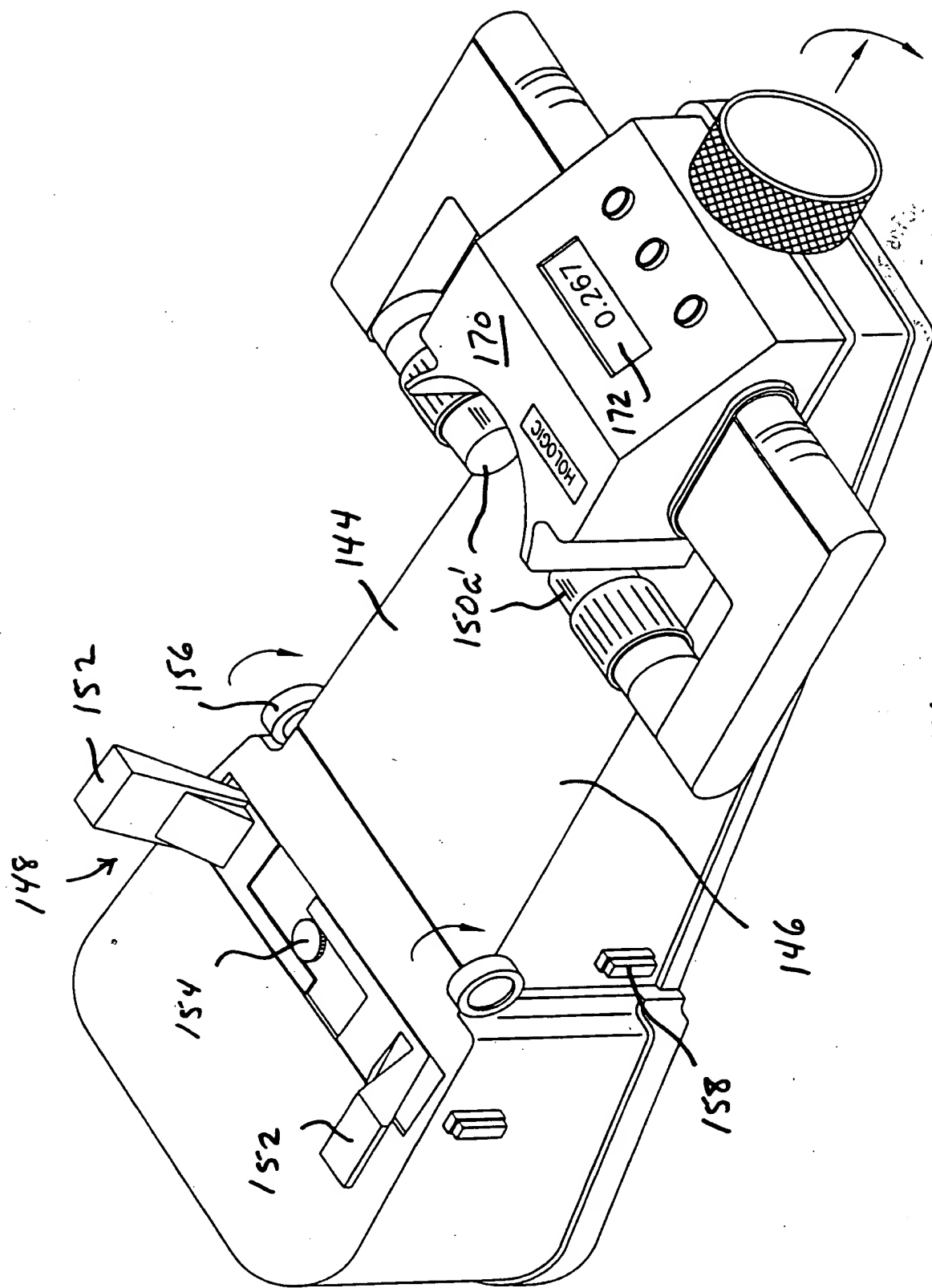


FIG. 14

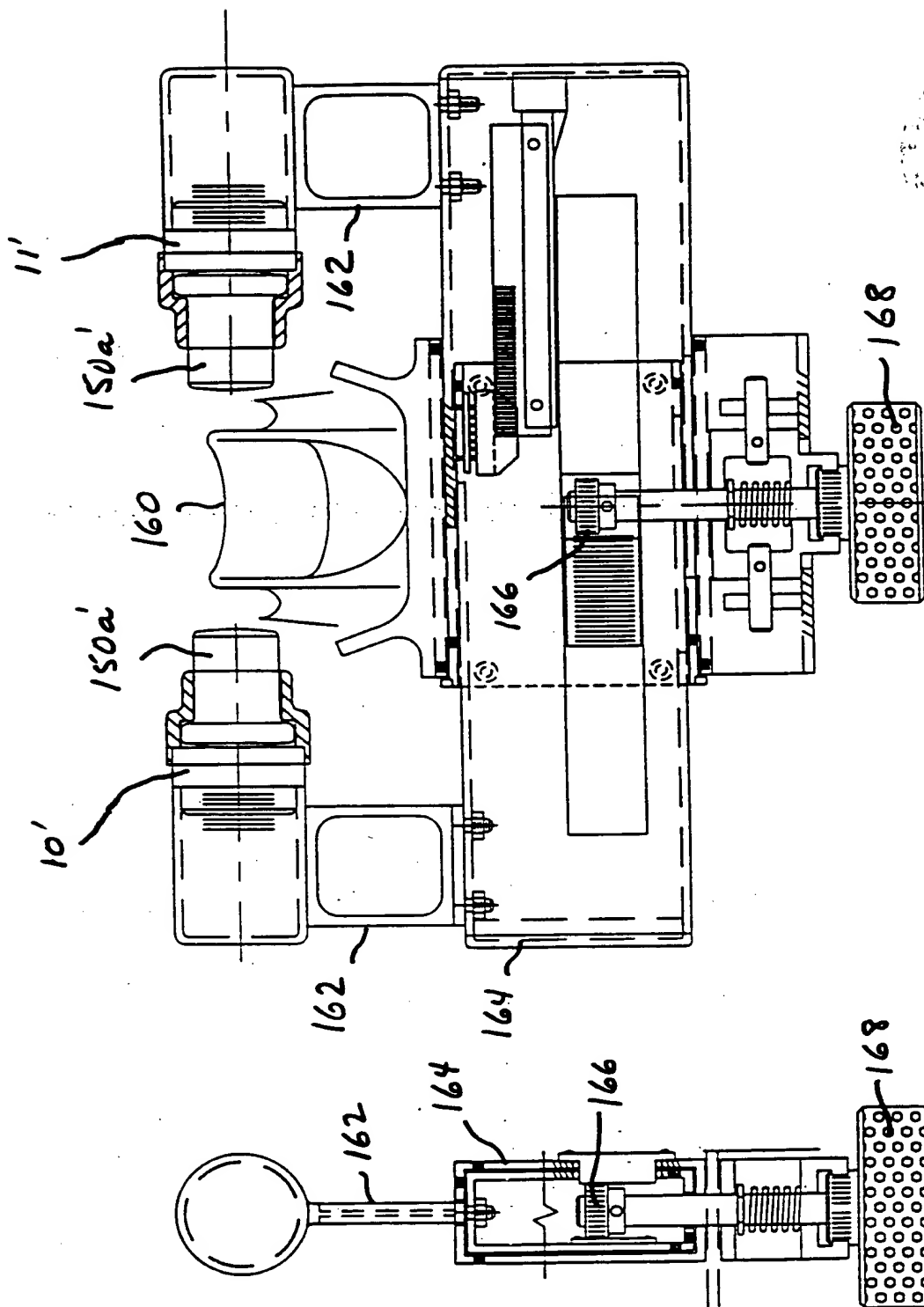


FIG. 15A

FIG. 15B

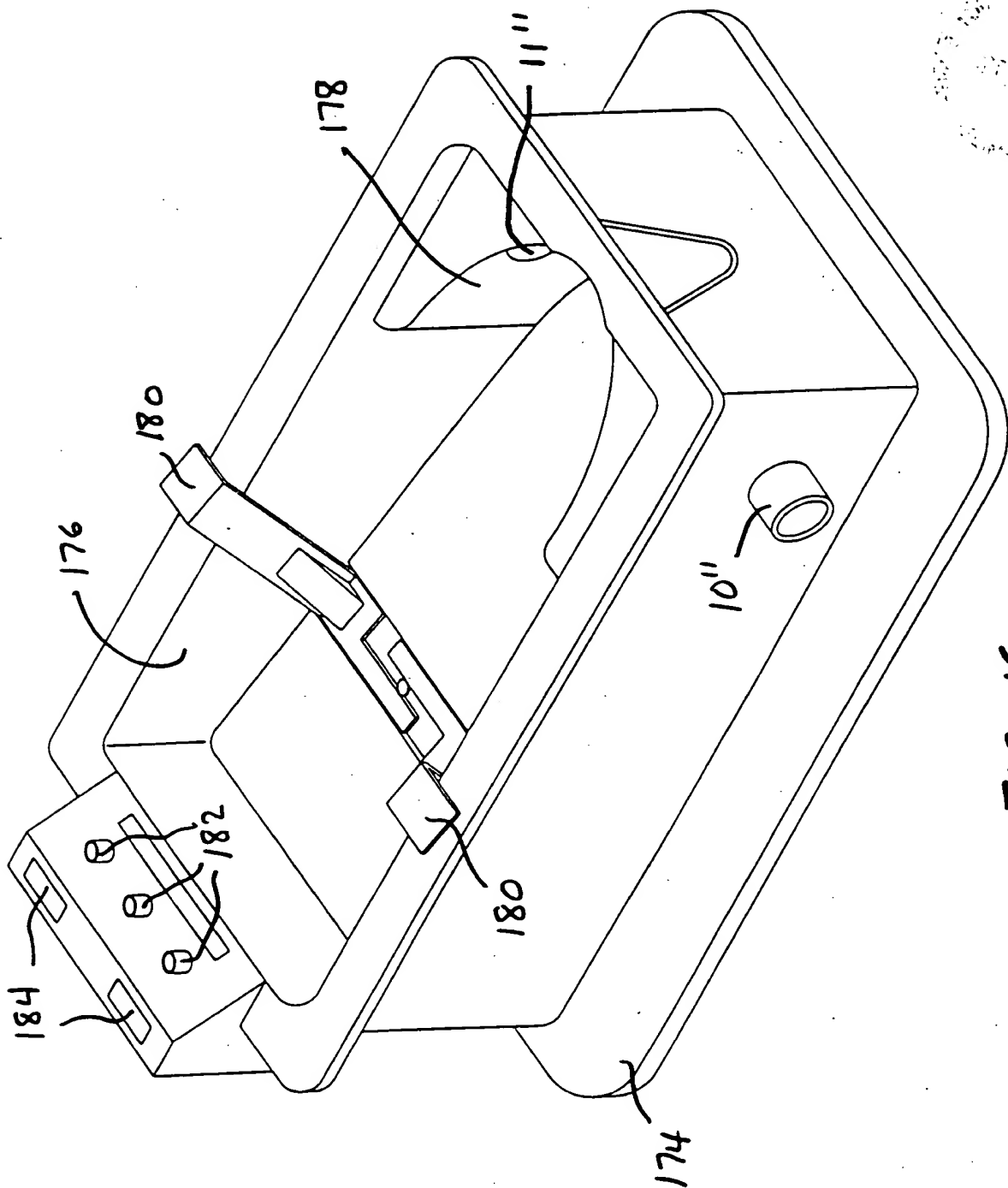


FIG. 16

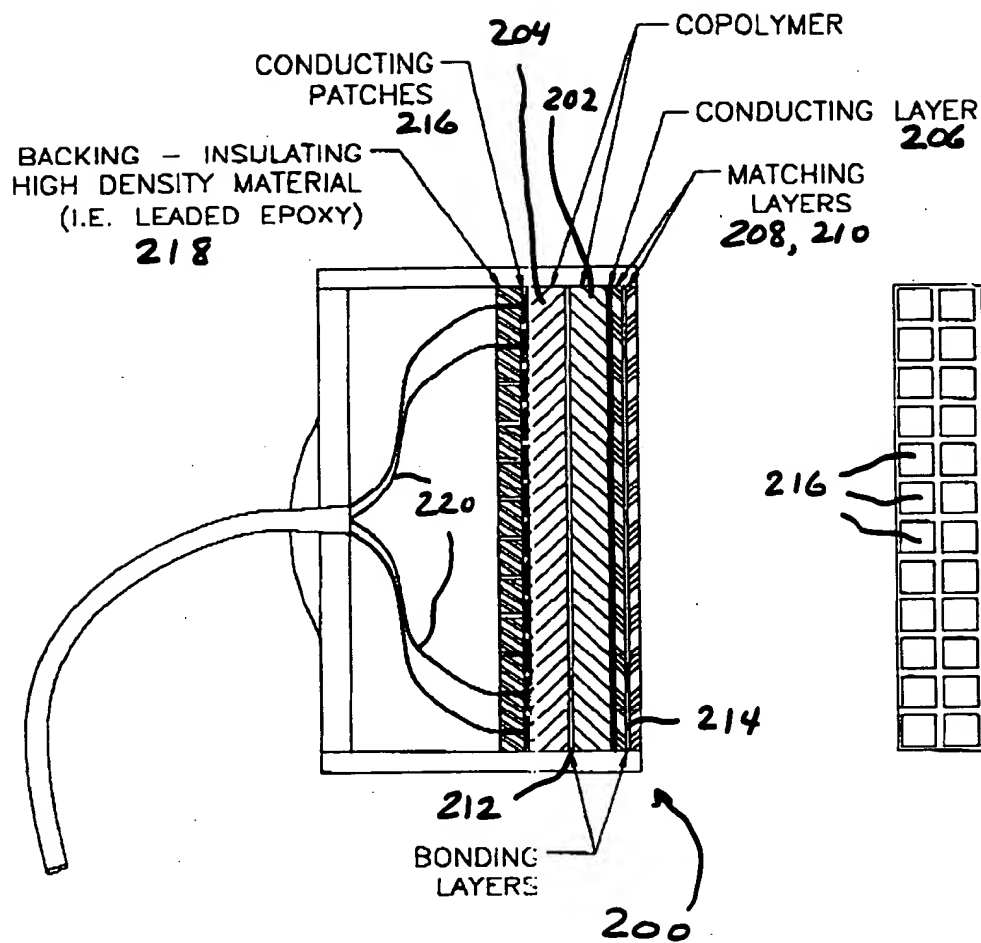


FIG. 17B

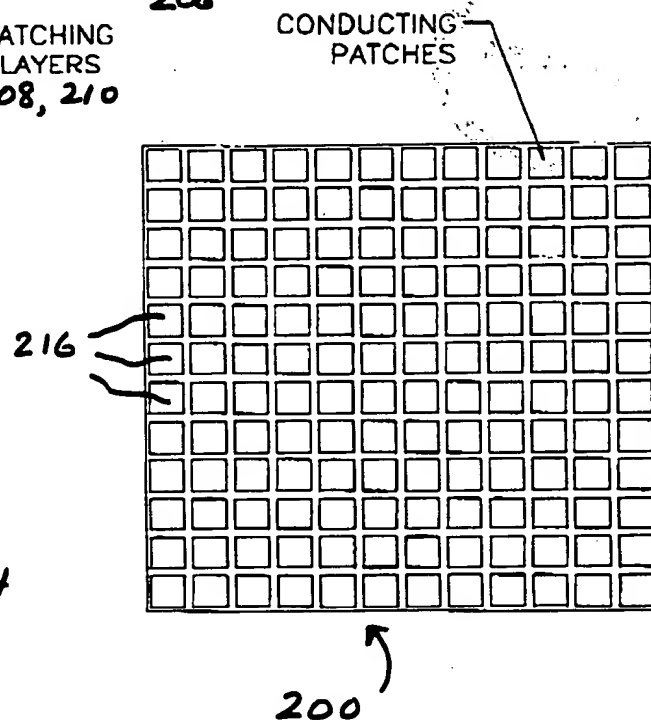


FIG. 17A

3910
20 10 10
10 20 10

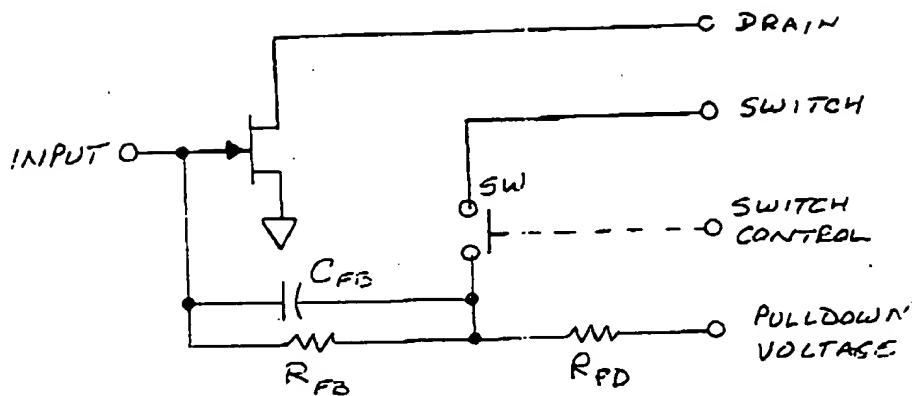


FIG. 18A N-Channel FET Input Stage

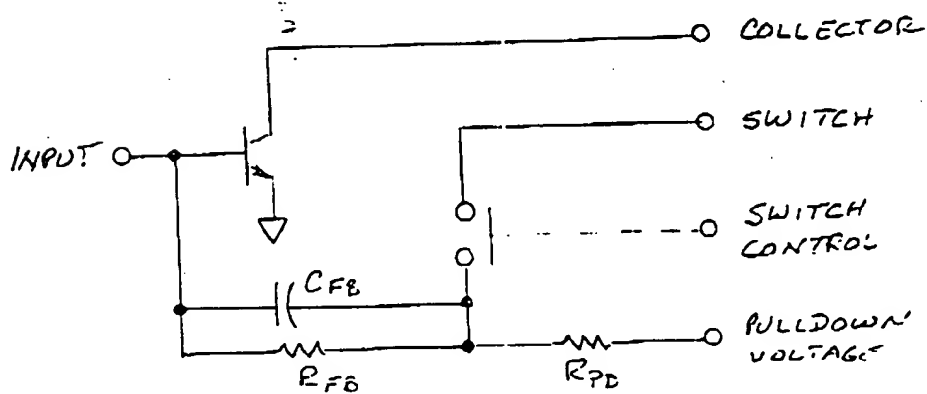


FIG. 18B NPN Transistor Input Stage

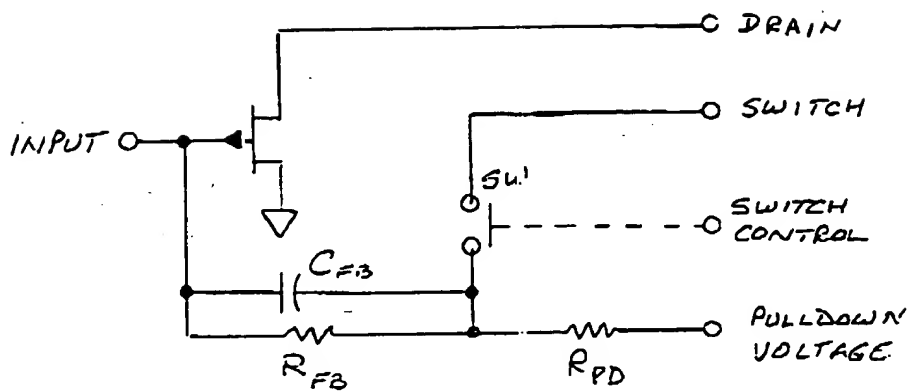


FIG. 18C - P-Channel FET Input Stage

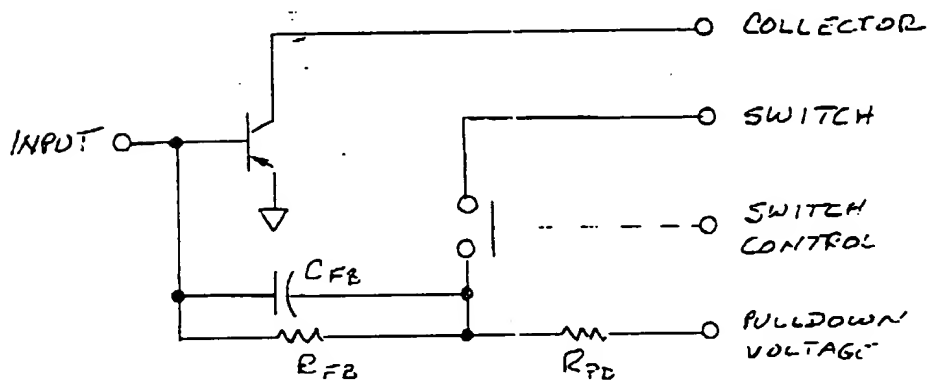


FIG. 18D - PNP Transistor Input Stage

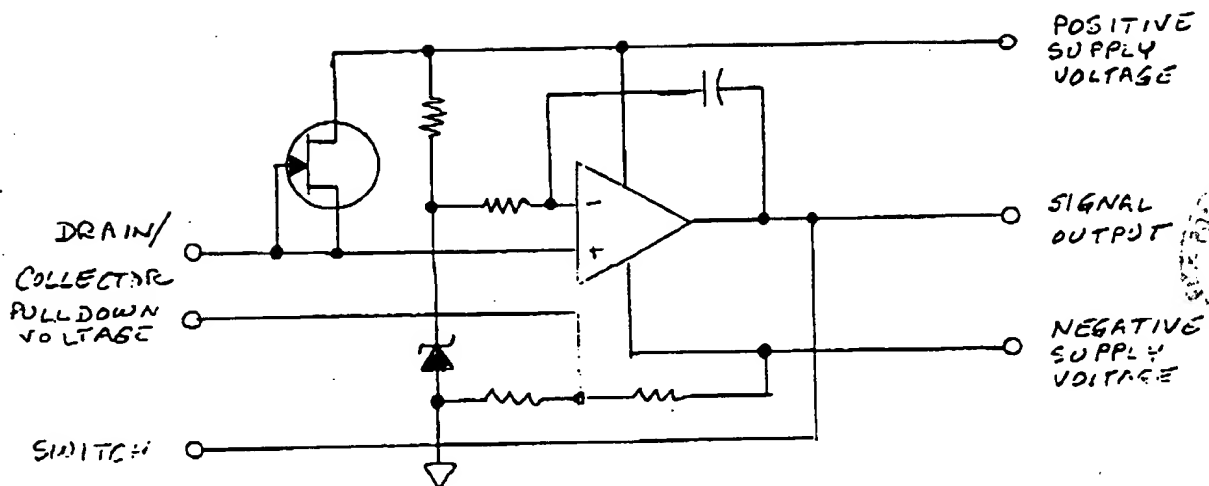


FIG 18E-- PREAMPLIFIED OUTPUT STAGE
FOR N-CHANNEL OR NPN INPUT STAGE

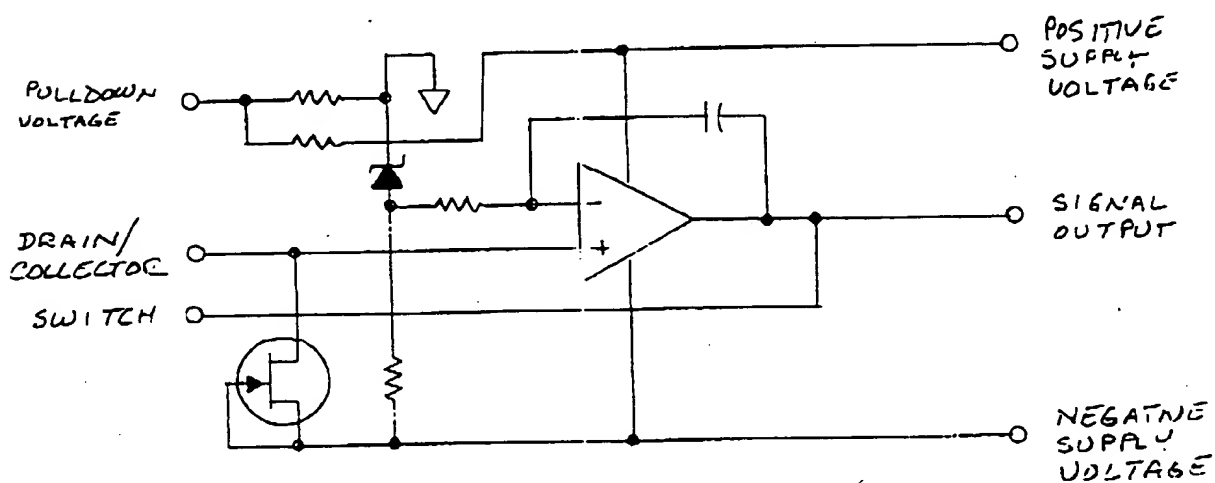


FIG. 18F-- PREAMPLIFIED OUTPUT STAGE
FOR P-CHANNEL OR PNP INPUT STAGE